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FORM PTO-1449 MODIFIED	Docket No.: 3020.02US02	Application No. 09/899,765
INFORMATION DISCLOSURE CITATION IN AN APPLICATION	APPLICANT: Meyer FILING DATE: July 5, 2001 GROUP ART UNIT: 2123	

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	4,792,913	Dec. 1988	Buckland et al.			
	4,985,860	Jan. 1991	Vlach			
	5,105,373	Apr. 1992	Rumsey et al.			
	5,297,066	Mar. 1994	Mayes			
	5,394,346	Feb. 1995	Milsom			
	5,471,409	Nov. 1995	Tani			
	5,481,484	Jan. 1996	Ogawa et al.			
	5,822,567	Oct. 1998	Takeuchi			
	5,991,522	Nov. 1999	Shoen			
	6,110,217	Aug. 2000	Kazmierski et al.			

EXAMINER SIGNATURE	DATE CONSIDERED
	1/19/03

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.
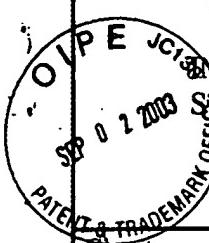
Substitute for form 1449/PTO				Complete if Known	
				Application Number	09/899,763
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				Filing Date	July 5, 2001
				First Named Inventor	Meyer
				Art Unit	2123
				Examiner Name	Not Assigned
Sheet	1	of	1	Attorney Docket Number	3020.02US02

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T[2]
✓		*Electronic Circuit Simulation in a Mixed-Language Environment*, Litovski et al., Microelectronics Journal, Mackintosh Publications Ltd., Vol. 29, No. 8, August 1, 1998; pgs. 553-558.	
✓		*Hardware Description Languages for ALECSIS Simulator*, Damnjanovic et al., Microelectronics 1995 Proceedings, New York, IEEE, September 1995, pgs. 525-528.	
✓		Verilog-AMS Language Reference Manual, Open Verilog International, December 1999, Los Gatos, California, Chapter 9.	
✓		*On the Design of Mixed-Mode Simulators for Modern VLSI Circuits*, Abdallah et al., Circuits and Systems Proceedings 1995, New York, IEEE, August 1995, pgs. 1168-1171.	
✓		*A System-Level Simulation Environment for System-on-Chip Design*, Schneider et al., 13th Annual IEEE International ASIC/SOC Conference, September 2000, Washington, D.C., pgs. 58-62.	
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